A Novel Digital Capacitor Charge Balance Control Algorithm with a Practical Extreme Voltage Detector

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***Abstract*—Dc-dc Buck converter has a major application for powering integrated circuit under stringent regulation, nowadays. In this paper, a practical digital control algorithm is presented to achieve the optimal response for dc-dc Buck converters without relying on the knowledge of the passive component value (inductance and capacitance). This algorithm introduces the curve fitting analysis for deriving the formulas to optimize the response under different transients from input voltage and load current. An opportunity is also provided for adaptive voltage positioning (AVP) technique under load transients without significant modifications on the original algorithm. Furthermore, an operational amplifier (OPAMP) based peak/valley voltage detector is introduced in place of using a fast or asynchronous ADC, upon which an improved performance and design simplicity can be expected on the entire digital control system. The estimation error of the proposed scheme is simulated and illustrated to provide a design guideline. Finally, simulation and experimental results are provided to validate the proposed schemes.**

***Index Terms*—Capacitor Charge Balance Controller, Digital Control, Dc-Dc Buck Converter, Extreme Voltage Detector, Optimal Control, AVP, Fast transient performance**

I. INTRODUCTION

The voltage regulation requirements for digital integrated circuits (ICs) power supplies are more and more stringent, that is, low output overshoot/undershoot and short settling time under increasingly large load transients or disturbances. So it becomes more and more difficult to meet the certain requirements using conventional linear mode controllers such as voltage and current mode controllers of which the design is normally made with the help of small signal model analysis. Due to the undesired voltage deviations, a large volume of output capacitance is always used which occupies more board area with linear mode controllers. To break the bandwidth barrier for faster transient response, couples of analog controllers and digital control algorithms have been introduced in some previous literatures to achieve this objective [1]-[9]. The capacitor charge balance concept is first introduced in [1] for achieving minimum voltage variations and settling time. Compared with analog controller, digital counterpart offers many advantages such as re-programmability, reliability, noise immunity, low sensitivity to ageing and environmental factors and simplicity of complex arithmetic. Also, the CBC controller can be easily implemented using digital signal processing devices, such as DSP and FPGA, so extensive work has been conducted in designing digital CBC controllers that further improves robustness [2]-[3], practical performance [6]-[9], [12] and simplicity of the control system. However, all the previous schemes cannot address at least one of the following limitations:

1. Complex real-time calculation is embedded in the algorithm, like division and square root [1], [3];
2. Current sensing information is needed to implement the proposed scheme for estimation, adding more cost to the controller and sacrificing the accuracy [5], [6];
3. Algorithm requires the knowledge of design parameters of passive components mounted in the switched mode power supply, which limits the practicality of the proposed scheme ;
4. Difficult or impossible to apply adaptive voltage positioning (AVP) using proposed schemes for powering modern processor such as Intel modules;
5. A fast or asynchronous analog to digital converter (ADC) [8] or certain type of active capacitor current sensor is required to detect the capacitor current zero-crossing time point [3], but degrading the cost-efficiency and robustness of the overall system [3], [8];

Another observation of the previous techniques is that in order to derive the formulas of the proposed algorithms, capacitor charge and discharge area associated with the inductor current is always selected as a starting or breakthrough point. But in this paper, a new curve fitting based derivation is discussed to provide a possibility for achieving parameter-independent control strategy under different transients. When a well-designed Buck converter has negligibly low *ESR* in the output capacitor, the proposed algorithm is parameter-independent and robust, which can be extended for AVP applications [8].

The paper is organized as follows. In Section II, the principles of the proposed optimal control algorithm for load current step transient is introduced. In Section III, the proposed extreme voltage detector is discussed to detect the output voltage peak/valley. In Section IV, the critical mathematical expressions of the proposed algorithm coupled with an estimation error analysis are derived and approximated for practical guidelines. The extension of the proposed scheme for optimizing the input voltage transient response is presented, followed by the hardware implementation diagrams in Section V. Finally, the simulations and experimental results are demonstrated in

Section VI to validate the proposed control algorithm.

II. Operating Principles of the Proposed CBC Control Algorithm

For all the controllers or schemes based on the capacitor charge balance principles [1]-[11], the time points t_1 when the output capacitor current undergoes zero-crossing and t_2 when the DPWM signal is switched, are very important to arrange the optimal control actions, accordingly (see Fig. 1). In this paper, a practical analog extreme voltage detector is presented to find t_1. And in place of calculating the time interval T_2 [1], [3]-[7], the time information t_2 is mapped to the switching point voltage (SPV) V_{SW}, which provides a unified formula set to the optimal algorithm for the transients from both the load current and input voltage. Also an extension can be made for AVP application based on simply modified SPV information. So in this section, the operating principles of the proposed scheme for load current transients are discussed.

Operations of the Proposed Digital CBC Controller under Load Current Step Transient Cases

For the load current step change cases, we can firstly sense the maximum/minimum output voltage at t_1 and the microprocessor will convert this information into SPV V_{SW} to detect t_2 by comparing V_{SW} with V_o. The main procedures of the control algorithm under negative current step (in CCM mode) are listed as follows for an example:

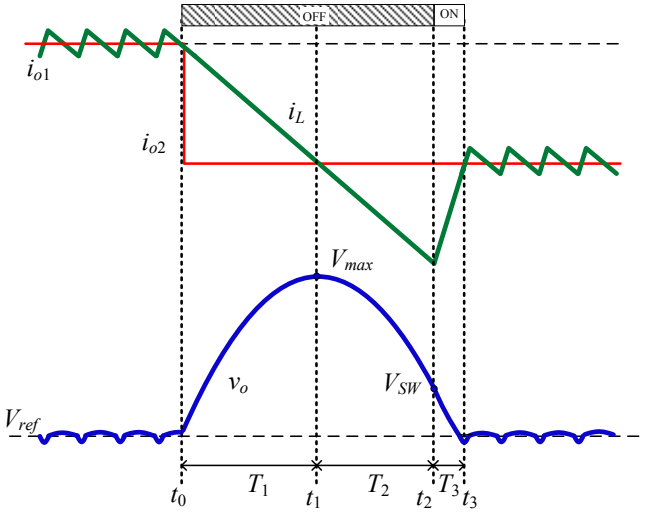

Fig. 1. Inductor current and capacitor voltage waveforms under negative current step change case.

1. Assuming that a load current transient happens at the time point t_0, and the output of the transient event detector will exceed its preset threshold band right away, triggering the optimal controller. And the proposed digital CBC controller DPWM output will be set to low;
2. After a short period of delay for blanking the transition noise such that the switching ringing will not degrade the performance of the extreme voltage detector, the voltage detector will be monitored by the microprocessor (DSP);
3. When the certificated output signal edge (rising edge) of the voltage detector is responded by the microprocessor as an external interrupt at t_1, the output voltage peak V_{max} will be sensed;
4. According to the maximum voltage V_{max}, the SPV V_{SW} can be easily calculated using DSP;
5. The DPWM will be reset to high when the output voltage reduces to V_{SW} at t_2;
6. At t_3, the output voltage recovers to the desired voltage V_{ref}, and the conventional PID controller is reactivated for output voltage regulation again.

For positive load transient case, the proposed controller can be operated similarly, but instead of sensing V_{max} and converting to V_{SW}, the minimum voltage V_{min} will be sampled for detecting t_2. Also, the DPWM sequence needs to be switched, that is, to high at t_0 and to low at t_2.

III. Operating Principles of the Proposed Practical Analog Extreme Voltage Detector and Its Hardware Implementation

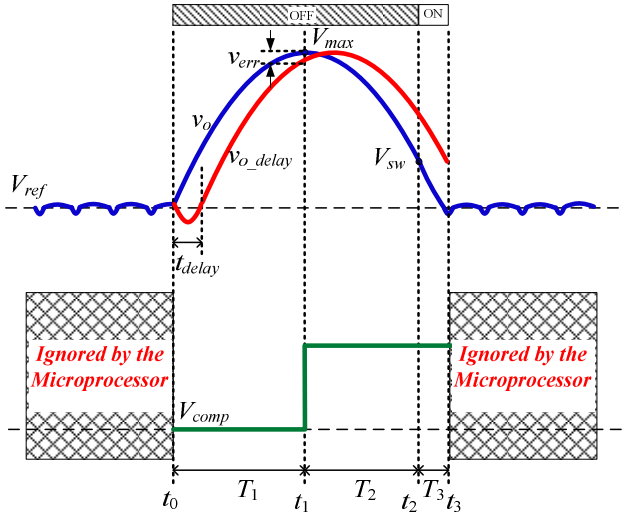

Fig. 2. Operating principles of the analog extreme voltage detector for negative load step tranisent case (V_{ref}: reference voltage; v_{err}: error between original signal and delayed signal; t_{delay}: time delay; v_{comp}: output voltage of the comparator)

A. An Analog Extreme Voltage Detector for Locating the Voltage Peak/Valley at t_1

Because of the sensor mismatching [3], cost and accuracy issues [8], a practical extreme voltage detector is presented in this paper. In Fig. 2, as an instance, during negative load current step transient, the output voltage overshoot is delayed with a period of time t_{delay}, and represented as v_{o_delay}. Then, the voltages v_o and v_{o_delay} will be fed to the input ports of a output comparator. And at a certain voltage error v_{err}, the comparator output signal begins rising to this upper limit, such that the maximum voltage and time point t_1 can be detected by the DSP (as an external interrupt).

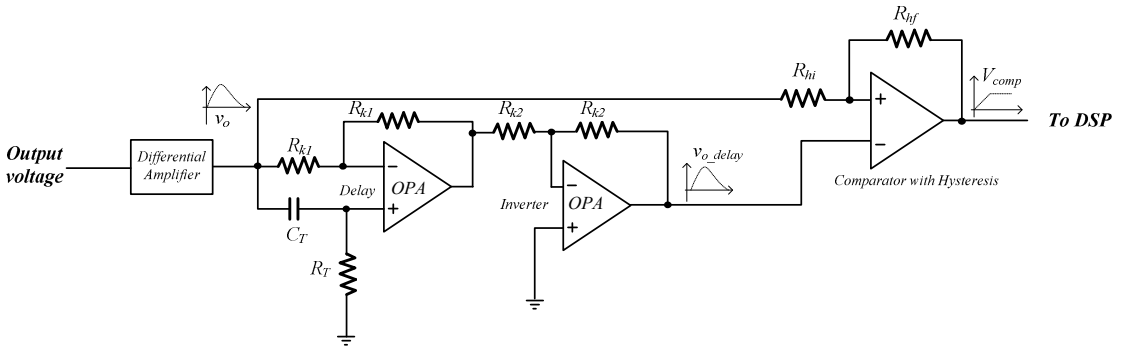

Fig. 3. Hardware implementation of the detector based on the adjustable delay circuit

Through proper design, v_{err} can be adjusted to 10mV-order by the inserted delay t_{dealy} and comparator hysteresis, such that the accuracy of the t_1 detection will be improved, compared with a common synchronous ADC [12], [13]. Since there is a finite *ESR* parasitizing in the output capacitor, the voltage peak/valley does not appear as it is expected but undergoes a period of lead time τ', which equals the product of *ESR* and output capacitance (i.e. $\tau'=ESR\cdot C$). So the inserted delay time t_{delay} can be compensated to a certain degree, with the help of this lead time (provided by *ESR*) and comparator hysteresis configuration (which can adjust the v_{err} band, see Fig. 2) In addition, the proposed voltage detector provides a flexibility for optimal tuning which will be discussed in the next section.

B. Hardware Implementation of the Proposed Analog Extreme Voltage Detector

In Fig. 3, an adjustable delay circuit is synthesized based on the Padé approximation (1).

$$\frac{v_{c\_delay}}{v_c}=e^{-\tau s}\approx\frac{1-\tau s/2}{1+\tau s/2}=\frac{1-R_TC_Ts/2}{1+R_TC_Ts/2} \tag{1}$$

In this circuit, the delay time constant τ can be adjusted by the product of R_T and C_T (i.e. $\tau=R_T\cdot C_T$). And the inverting section is added to the output end to implement two-fold functions: inverting the delayed signal and tuning the output voltage offset level. The output comparator is connected with a hysteresis configuration and the one with latched output function is more preferred for blanking steady-state comparison output "noise", such as TL3016 (TI Company) [15]. Also, in the experiments, the aforementioned delay can be also compensated by using a trim resistor as the feedback resistor to tune the delayed voltage v_{o_delay} offset level such that the crossover of the two voltage waveforms (v_o and v_{o_delay}, see Fig. 2) will appear at t_1.

IV. Mathematical Derivations of the Proposed Algorithm and Estimation Error Analysis

A. Estimation of the Switching Point Voltage (SPV) Based on Curve Fitting

For the microprocessor voltage regulators (VRs), sufficiently large output capacitance is added to suppress the output voltage deviation. And also because of the low voltage rating, often, the selected ceramic capacitor will appear very low *ESR*. So in the following discussion, an ideal dc-dc Buck converter model is used. In this paper, derivations for negative current transient is shown as an example (in Fig. 1) to explain how to compute the SPV V_{SW} based on curve fitting analysis.

For negative current step change, during the time period t_1-t_2 and t_2-t_3 the capacitor current can be approximated as a linear function in (2) and (3), where m_1 ($m_1=V_{in}-V_o/L$) and m_2 ($m_2=V_o/L$) are the rising and falling slew rates of the inductor current. As an alternative approach for solving differential equations, the output/capacitor voltage can be approximated with a parabolic curve based on the linear output capacitor current in (2) and (3).

$$i_C(t)\big|_{t_1\sim t_2}=-m_2(t-t_1)=-\frac{V_o}{L}(t-t_1) \tag{2}$$

$$i_C(t)\big|_{t_2\sim t_3}=m_1\left(t-t_3+\frac{1}{2}DT_s\right)=\frac{V_{in}-V_o}{L}\left(t-t_3+\frac{1}{2}DT_s\right) \tag{3}$$

So the SPV voltage V_{SW} can be calculated using (4), where the symbol T_s represents the switching period and the V_{ref} is for the output voltage reference, while the equation (5) provides the formula for computing the maximum voltage $V_{\max}$ at t_1.

$$V_{SW}=\frac{1}{2C}m_1\left[T_3^2-\left(\frac{1}{2}DT_s\right)^2\right]+V_{ref} \tag{4}$$

$$V_{\max}=\frac{1}{2C}m_2T_2^2+V_{SW} \tag{5}$$

Without sacrificing the accuracy of the algorithm a lot, especially when the switched-mode power supply operates at a high frequency and narrow duty ratio (12 V-1.5 V), the item $(1/2DT_s)^2$ can be omitted in the equation (4). Therefore, the voltage V_{SW} can be fitted as (6) based on the two known data points (t_1, $V_{\max}$) and (t_3, V_{ref}). When the output voltage falls down to V_{SW}, we set the DPWM to high.

$$V_{SW}=\frac{m_2(V_{\max}-V_{SW})}{m_1}+V_{ref}=\frac{V_o}{V_{in}}V_{\max}+\frac{(V_{in}-V_o)}{V_{in}}V_{ref}=DV_{\max}+(1-D)V_{ref} \tag{6}$$

For positive load current step, the SPV can be similarly derived as (7). Another unique merit of the proposed algorithm is that for input transients the same equation set is valid, that is, equation (6) can be used for positive input voltage change and equation (7) is applicable for negative

input voltage transient. In conclusion, according to the derivations discussed above, in the algorithm, neither inductor nor capacitor value is explicit in the equations (6) and (7). Also, the computation is only based on voltage information.

$$V_{SW} = V_{ref} + \frac{m_2\left(V_{\max} - V_{SW}\right)}{m_1} = \frac{V_o}{V_{in}}V_{ref} + \frac{\left(V_{in} - V_o\right)}{V_{in}}V_{\min} = DV_{ref} + (1-D)V_{\min} \quad (7)$$

Furthermore, if we modify the V_{ref} definition to the adaptive voltage position V_{ref}-R_{droop}·ΔI (R_{droop} is the droop resistance), this algorithm can be extended to AVP applications in (8) for negative load transient and (9) for positive load transient.

$$V_{SW} = DV_{\max} + (1-D)\left(V_{ref} - R_{droop}\cdot\Delta I\right) \quad (8)$$

$$V_{SW} = D\left(V_{ref} - R_{droop}\cdot\Delta I\right) + (1-D)V_{\min} \quad (9)$$

B. *Estimation Error of the SPV V_{SW}*

To investigate the effects of the *ESR* value and the switching frequency on the SPV estimation error of the proposed algorithm, simulation results are illustrated in Fig. 4 under 10 A positive and negative current step transient conditions. The large error of the *SPV* will deteriorate the performance of the proposed controller because of the wrong timing t_2 and cause the ring-back problem [3]. However, with a relatively high switching frequency (≥100 *k*Hz) and low *ESR* (≤1 *m*Ω), the proposed algorithm exhibits a good accuracy with less than 2.5% error whose impact is negligible on the overall transient performance.

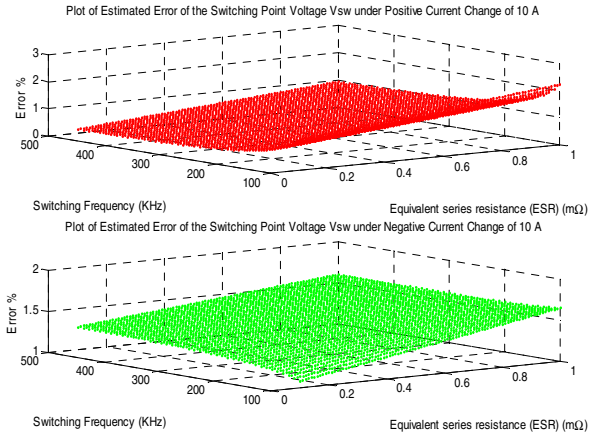

Fig. 4. Estimation error of the switching point voltage (SPV) Vs. ESR/switching frequencies under positive load step change of 10 A (in red) and negative load step change of 10 A (in green)

V. The Extension of the Proposed Digital CBC Controller for Optimizing Input Voltage Transient Response and the Implementation of the Digital Control System

A. *Operations of the Proposed Digital CBC Controller under Input Voltage Transient Cases*

The two-switching-cycle compensation algorithm proposed in [2] has several drawbacks, such as, losing its applicability for the ultra-fast/large input voltage change scenarios (≥ 2.5 V) and requiring accurate design component value (*L* and *C*) and current sensing information to calculate the formulas to control the converter. However, the proposed algorithm can be also applied to the ultra-fast/large transient cases, without depending on any knowledge of passive components value or current sensing information.

Although the input voltage transient slew rate is always limited by the input filter which in fact weakens the practicability and advantage of the CBC controller for improving input voltage transient cases, it is definitely a unique feature for the proposed algorithm to solve both of the transient cases from input and output sides. Similarly, the main procedures of the proposed algorithm under negative input voltage transient are explained below:

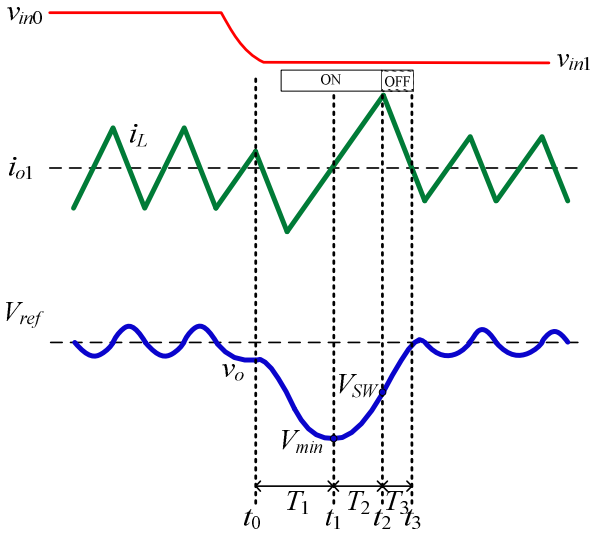

Fig. 5. Inductor current and capacitor voltage waveforms under negative voltage step change case

1. Assuming that an ultra-fast negative input voltage step transient ends at the time point t_0, and the transient event detector output will trigger the optimal controller, immediately. And the proposed digital CBC controller DPWM output will be set to high;
2. After a short period of delay for blanking the transition noise, the extreme voltage detector will be monitored by the DSP;
3. When the falling edge of the voltage detector is responded by the DSP as a external interrupt at t_1, the output voltage will be sampled by the ADC;
4. The CBC controller will calculate the V_{SW} where the DPWM will be set to low (at t_2);
5. At t_3, the output voltage recovers to the desired voltage V_{ref}, and the conventional PID controller is reactivated for output voltage regulation.

For positive input voltage transient case, the proposed controller can be operated similarly, but instead of sensing the voltage valley $V_{\min}$ and converting to V_{SW}, $V_{\max}$ will be

sampled for determining t_2. Also, the DPWM sequence needs to be changed, that is, to low after t_0 and to high at t_2.

B. *Hardware Implementation Diagram of the Proposed Digital Control System*

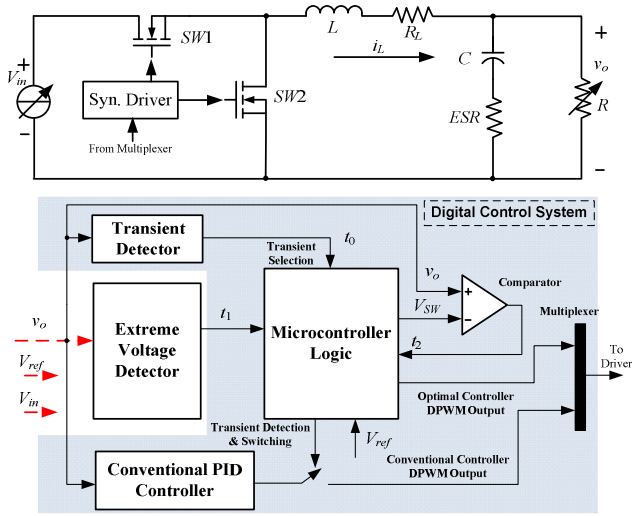

Fig. 6. Hardware implementation diagram of the digital control system

The hardware implementation diagram is illustrated in Fig. 6. No current sensing signal is required in this system. And at most two voltage sensors are used to collect the instant information of the input voltage (V_{in} for input voltage transient only) and output voltage (v_o). The transient detector in the proposed scheme is implemented by monitoring the output voltage (for input voltage transient) and the equivalent capacitor current (for load transient). The time point t_1 is determined by using the aforementioned analog extreme voltage detector. The digital comparator is for detecting t_2 and the multiplexer mixes the CBC signal with the PID DPWM signal. At the end, a synchronous buck converter driver will create the driving signal to the switches *SW1* and *SW2*.

VI. Simulations and Experimental Verifications

A. *Simulation Results*

In order to verify the functionalities of the proposed optimal algorithm, a dc-dc Buck converter model undergoing different transient conditions is simulated. And the simulated results are shown in Fig. 7 and Fig. 8. The design parameters are listed as follows in the Table 1. And for load transient cases, the input voltage is 12 V, while, for input voltage transient cases, the load current is 10 A.

Table 1: Design Parameters of the Dc-Dc Buck Voltage Regulator Module

V_o	Output Voltage	1.5 V
f_s	Switching Frequency	350 kHz
L	Output Filter Inductance	1 μH
R_L	DC Resistance of the Inductor	1 $m\Omega$
C	Output Filter Capacitance	180 μF
ESR	Equivalent Series Resistance	0.5 $m\Omega$
ESL	Equivalent Series Inductance	100 pH

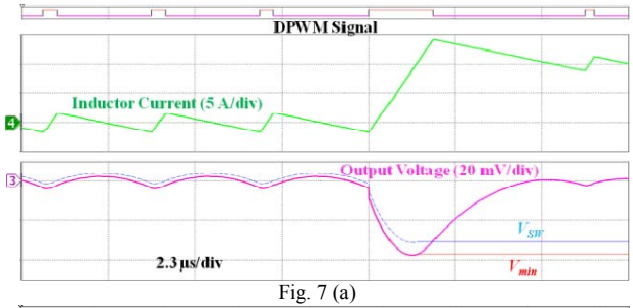

Fig. 7 (a)

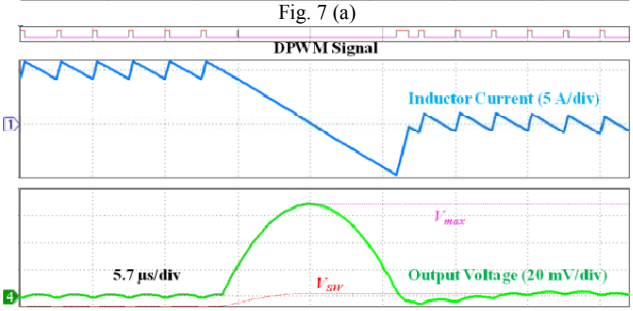

Fig. 7 (b)

Fig. 7. Simulation results of the dc-dc Buck converter following current transient (a) positive step 0 A→10 A; (b) negative step 10 A→0 A

From Fig. 7 (a) and (b), we can observe the similar response waveforms to those in the previous sections by theoretical analysis using proposed CBC controller. SPV V_{SW} is shown in each of the cases for reference. Under a 10 A load transient, the voltage deviation is 35 mV for positive step and 185 mV for negative step, while, the setting time is 4 μs for positive case and 14.5 μs for negative case, respectively.

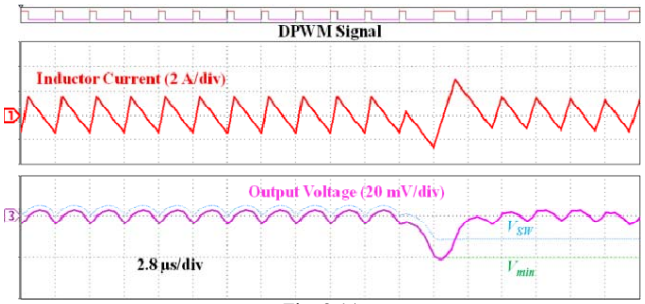

Fig. 8 (a)

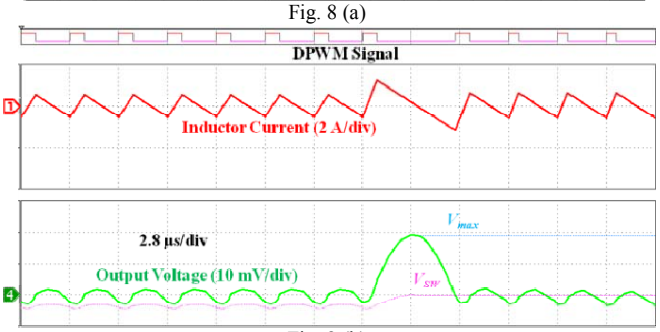

Fig. 8 (b)

Fig. 8. Simulation results of the dc-dc Buck converter following input voltage transient (a) negative step 7.5 V→ 5 V; (b) positive step 5 V→7.5 V

An ultrafast input voltage step transient of 2.5 V is also simulated to verify the equations presented in the Section III.

Without any necessary modifications (mentioned in previous literatures [2]), the proposed algorithm is also applicable for regulating the input voltage transients. In Fig. 8, the undershoot is 22 mV with 7 μs settling time for negative input voltage transient, while, under positive input voltage transient, the overshoot is 18 mV with 6μs recovery time.

Also for comparison, a well-design PID controller (bandwidth: ≈75 *k*Hz, Phase margin ≈60 °) is also simulated for regulating the dc-dc buck VRM shown in Fig. 9 and Fig. 10. The PWM signals are shown for the comparison between proposed CBC controller (sw_CBC) and linear voltage mode controller (sw) in the top section. The inductor current (iL) and output voltage waveforms (vo) are also simulated with two types of controller shown on the bottom.

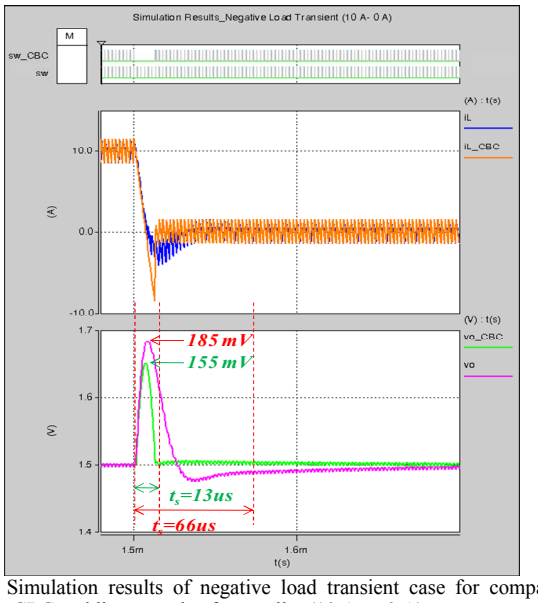

Fig. 9. Simulation results of negative load transient case for comparison between CBC and linear mode of controller (10 A -> 0 A)

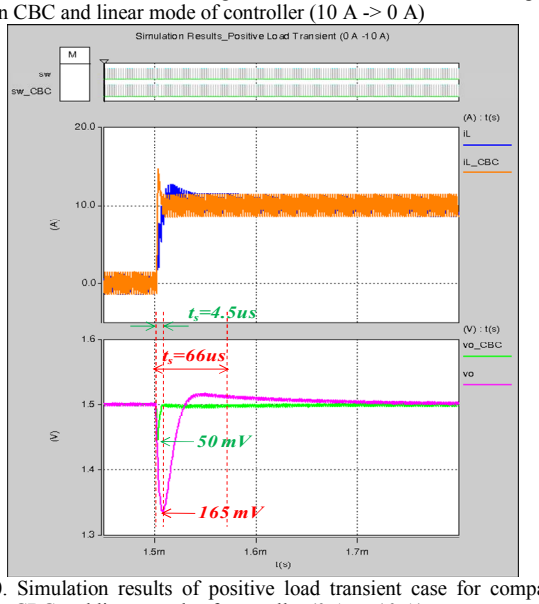

Fig. 10. Simulation results of positive load transient case for comparison between CBC and linear mode of controller (0 A -> 10 A)

To sum up, under the load transient cases, for negative step, the overshoot is reduced by 16% and settling time is shortened by 80%, while for positive step, the voltage undershoot is suppressed by 70% and settling time is improved by 93%. Notice that the difference between Fig. 7, Fig. 9 and Fig. 10 is caused by the different transient timing.

B. Design Prototype and Experimental Results

A 12 V-1.5 V prototype is designed using the same parameters in the simulation and a fixed-point 32-bit MCU TMS320F28027 is employed to implement the proposed CBC control algorithm, which is shown in Fig. 11.

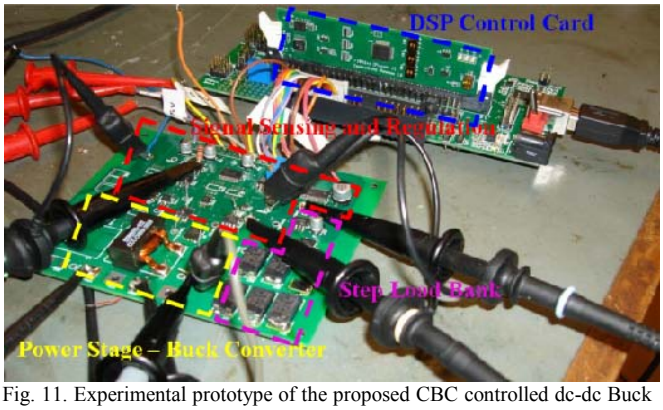

Fig. 11. Experimental prototype of the proposed CBC controlled dc-dc Buck converter

Experimental results, shown in Fig. 12 and Fig. 14, demonstrate the transient performance of conventional linear voltage mode controller (bandwidth: ≈75 *k*Hz, Phase margin ≈60 °) under the load current step change between no load (0 A) and full load (10 A). Limited by the bandwidth, the linear voltage mode controller will cause larger voltage variations and longer recovery time. For positive load transient, the voltage undershoot is about 170 mV with 61 μs settling time, while, the overshoot is about 185 mV with 56 μs settling time. Notice that the difference between Fig. 7, Fig. 9 and Fig. 10 is caused by the different transient timing.

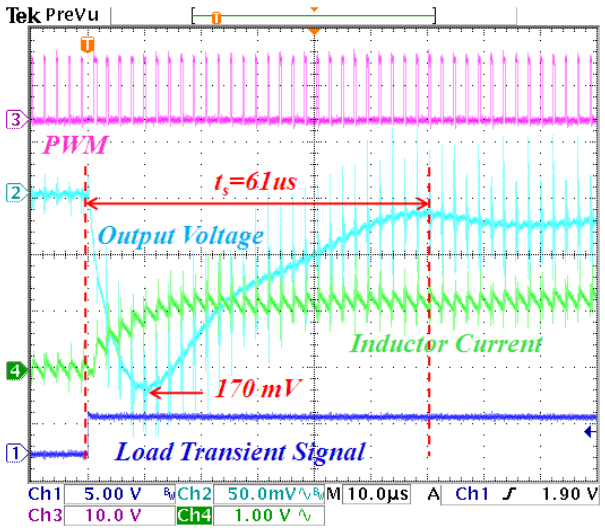

Fig. 12. Experimental results of positive load transient case 0 A- 10 A using linear mode controller

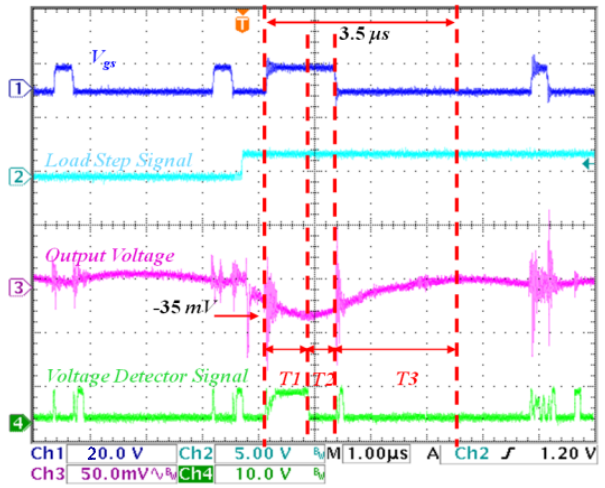

Fig. 13. Experimental results of positive load transient case 0 A- 10 A using CBC controller

Experimental results of proposed digital CBC controller are shown in Fig. 13 and Fig. 15, under the load current step change between no load (0 A) and full load (10 A). The proposed digital CBC controller demonstrates quite similar improved performance as its analog counterpart [3] but avoiding the sensor mismatching problem. In the experimental results, following the load transient cases, for negative step, the converter overshoot is reduced by 3% and settling time is shortened by 76%, while for positive step, the converter voltage undershoot is suppressed by 79% and settling time is improved by 94%.

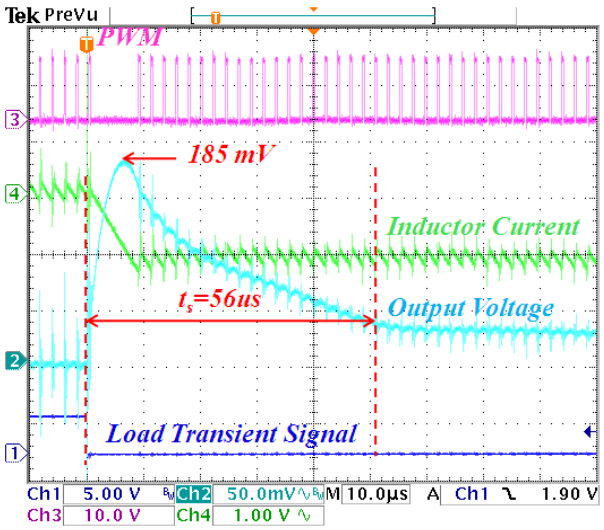

Fig. 14. Experimental results of negative load transient case 10 A- 0 A using linear mode controller

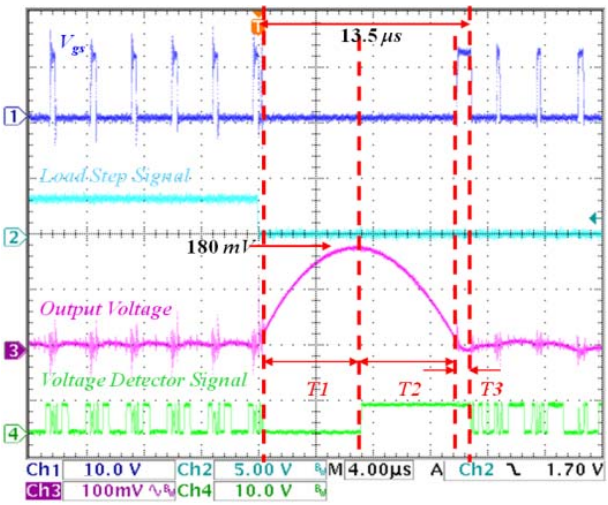

Fig. 15. Experimental results of negative load transient case 10 A- 0 A using CBC controller

Unluckily, experiments of the proposed digital CBC controller for improving ultrafast input voltage transient are hard to implement due to the limitations of the input filter and the power source.

VII. CONCLUSIONS

In this paper, an extreme voltage detector is employed to detect the critical time point t_1 and SPV concept is applied to design the CBC controller based on curve fitting analysis. It is demonstrated through simulations and experimental results, that the proposed parameter-independent algorithm can be implemented for low-*ESR* designed Buck converter to optimize the transient response performance. Through the comparison experiments, under the load transient cases, for negative step, the converter overshoot is reduced by 3% and settling time is shortened by 76%, while for positive step, the voltage undershoot is suppressed by 79% and settling time is improved by 94%. Also a possibility is shown for AVP

applications using this scheme without increasing algorithm complexity.

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